CY2300

Phase-Aligned Clock Multiplier

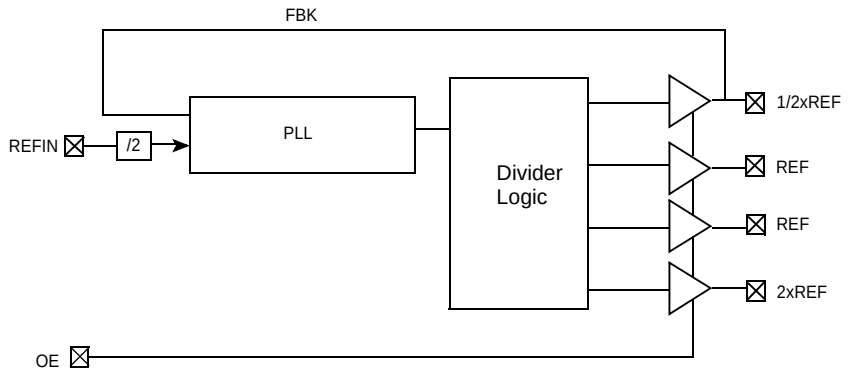
Features

- 4-multiplier configuration
- Single phase-locked loop architecture
- Phase Alignment
- Low jitter, high accuracy outputs
- Output enable pin
- 3.3V operation
- 5V Tolerant input
- Internal loop filter
- 8-pin 150-mil SOIC package
- Commercial Temperature

Benefits

- 1/2x, 1x, $\overline{1x}$, 2x Ref
- 10 MHz to 166.67 MHz operating range (reference input from 20 MHz to 83.33 MHz)
- All outputs have a consistent phase relationship with each other and the reference input
- Meets critical timing requirements
- Enables design flexibility and lower power consumption
- Supports industry standard design platforms
- Allows flexibility on Reference input
- Alleviates the need for external components
- Industry standard packaging saves on board space
- Suitable for wide spectrum of applications

Logic Block Diagram



Pinouts

Figure 1. CY2300 - 8-pin SOIC - Top View

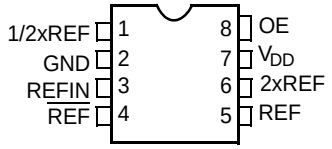


Table 1. Pin Definitions

Pin	Signal[1]	Description
1	1/2xREF	Clock output, 1/2x Reference
2	GND	Ground
3	REFIN	Input Reference frequency, 5V tolerant input
4	$\overline{\text{REF}}$	Clock output $\overline{\text{Reference}}$
5	REF	Clock output Reference
6	2xREF	Clock output, 2x Reference
7	VDD	3.3V Supply
8	OE	Output Enable (weak pull up)

Functional Description

The CY2300 is a 4-output 3.3V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part allows the user to obtain 1/2x, 1x, $\overline{1x}$ and 2x REFIN output frequencies on respective output pins.

The part has an on-chip PLL which locks to an input clock presented on the REFIN pin. The input-to-output skew is guaranteed to be less than ±200 ps, and output-to-output skew is guaranteed to be less than 200 ps.

Multiple CY2300 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.
The CY2300 is available in commercial temperature range.

Maximum Ratings

Supply Voltage to Ground Potential.....–0.5V to +7.0V

DC Input Voltage (Except Ref) ..... –0.5V to V_{DD} + 0.5V

DC Input Voltage REF ..... –0.5 to 7V

Storage Temperature ..... –65°C to +150°C

Junction Temperature..... 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, Fout < 133.33 MHz		18	pF
	Load Capacitance,133.33 MHz < Fout < 166.67 MHz		12	pF
C_{IN}	Input Capacitance		7	pF
t_{PU}	Power up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Note
1. Weak pull down on all outputs.

Electrical Characteristics

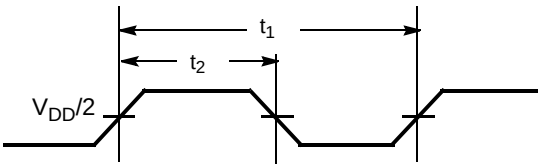
Parameter	Description		Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		100	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		50	µA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA		0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = –8 mA	2.4		V
I_{DD}	Supply Current	Unloaded outputs, REFIN = 66 MHz		45	mA
		Unloaded outputs, REFIN = 33 MHz		32	mA
		Unloaded outputs, REFIN = 20 MHz		18	mA

Switching Characteristics

Parameter	Name	Test Conditions	Min	Typ.	Max	Unit
$1/t_1$	Output Frequency	18-pF load	10		133.33	MHz
		12-pF load			166.67	MHz
	Duty Cycle[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t_3	Rise Time[3]	Measured between 0.8V and 2.0V			1.20	ns
t_4	Fall Time[3]	Measured between 0.8V and 2.0V			1.20	ns
t_5	Output to Output Skew on rising edges[3]	All outputs equally loaded Measured at $V_{DD}/2$			200	ps
t_6	Delay, REFIN Rising Edge to Output Rising Edge[3]	Measured at $V_{DD}/2$ from REFIN to any output			±200	ps
t_7	Device to Device Skew[3]	Measured at $V_{DD}/2$ on the 1/2xREF pin of devices (pin 1)			400	ps
t_J	Period Jitter[3]	Measured at Fout=133.33 MHz, loaded outputs, 18-pF load			±175	ps
t_{LOCK}	PLL Lock Time[3]	Stable power supply, valid clocks presented on REFIN			1.0	ms

Switching Waveforms

Figure 2. Duty Cycle Timing



Notes
2. Parameter is guaranteed by design and characterization. It is not 100% tested in production.
3. All parameters are specified with equally loaded outputs.

Switching Waveforms (continued)

Figure 3. All Outputs Rise/Fall Time

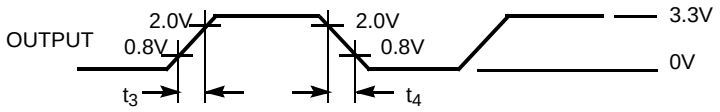


Figure 4. Output-Output Skew

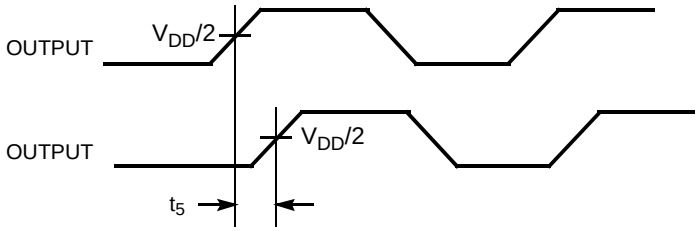


Figure 5. Input-Output Propagation Delay

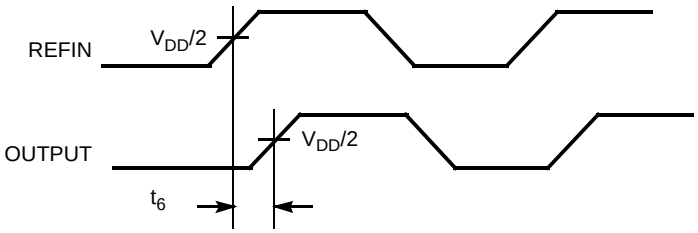
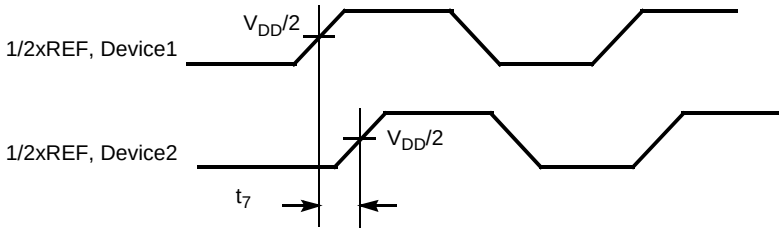
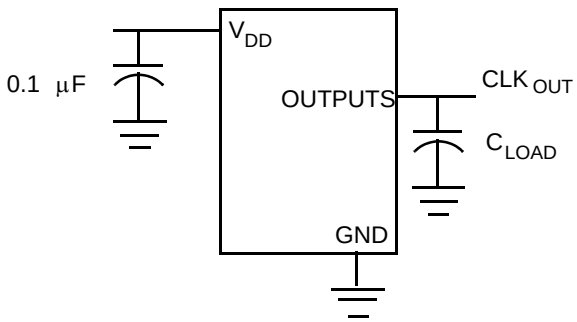


Figure 6. Device-Device Skew



Test Circuits

Test Circuit # 1

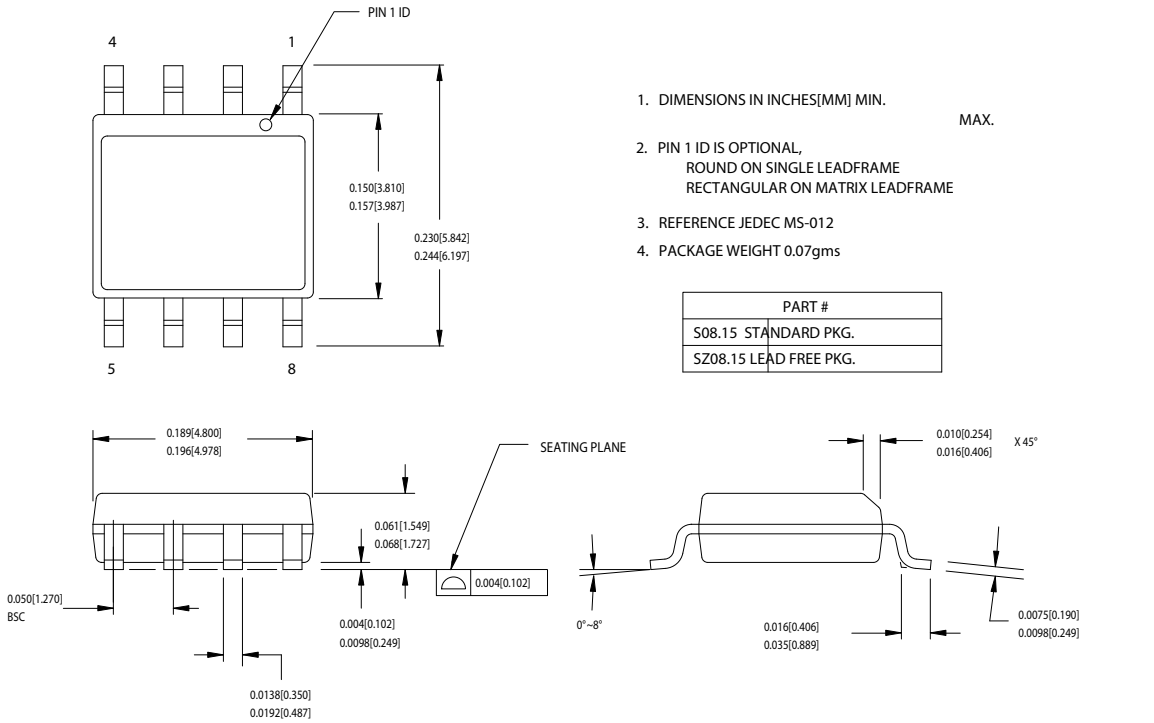


Ordering Information

Ordering Code	Package Type	Operating Range
Pb-Free		
CY2300SXC	8-pin 150-mil SOIC	Commercial
CY2300SXCT	8-pin 150-mil SOIC - Tape and Reel	Commercial

Package Drawing and Dimensions

Figure 7. 8-Pin (150-Mil) SOIC S8



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Document History Page

Document Title: CY2300 Phase-Aligned Clock Multiplier Document Number: 38-07252				
REV.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110517	SZV	01/07/02	Change from Spec number: 38-01039 to 38-07252
*A	121854	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*B	246829	RGL	08/02/04	Added Lead Free Devices
*C	2568533	AESA	09/23/08	Updated template. Removed Selector Guide. Removed Operating Conditions for CY2300SI Industrial Temperature Devices. Removed Electrical Characteristics for CY2300SI Industrial Temperature Devices. Removed Switching Characteristics for CY2300SI Industrial Temperature Devices. Removed part number CY2300SC, CY2300SC, CY2300SI, CY2300SI, CY2300SXI and CY2300SXIT.

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